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IN THE CLAIMS

Please cancel Claims 1-5, 14-20, 25-32, and 44-52 without prejudice, amend Claims 37, 38, 39, 40, and 43, and add new Claims 53-63 as follows:

5 1.-36 (Canceled)

37. (Currently amended) An ~~extensible~~ extended and user-configured pipelined digital RISC processor having an instruction set comprising a plurality of instructions comprising a base instruction set and at least one extension instruction, at least one of said base instruction set instructions or extension instructions comprising a branch instruction having a
10 plurality of user-configurable modes determined by a plurality of bits controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline, each of said modes being constrained to only one of a plurality of unique combinations of said plurality of bits.

38. (Currently amended) An ~~extensible~~ extended and user-configured pipelined
15 digital RISC processor having an instruction set comprising a plurality of instructions forming a base instruction set and at least one extension instruction, at least one of said instructions comprising a branch instruction including two data bits defining four discrete modes controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline;

20 wherein said execution is controlled without regard to a branch direction metric.

39. (Currently amended) An ~~extensible~~ extended and user-configured pipelined digital RISC processor having an instruction set, said processor comprising:

a processor core configuration including a base instruction set; and

25 at least one user-configured extension instruction within said instruction set, said at least one extension instruction comprising a branch instruction having at least one mode controlling the execution of at least one instruction in a delay slot following said branch instruction within said pipeline using a plurality of data bits, at least one of the particular combinations of data bits and the logical functions associated therewith being adapted for assignment by a user.

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40. (Currently amended) An extensible and user-configurable pipelined digital RISC processor design having base and extension instruction sets, at least one instruction within said base set comprising a branch instruction having ~~at least~~ four discrete modes for controlling the execution of at least one instruction in a delay slot following said branch instruction within
5 said pipeline, said processor design comprising:

a processor core configuration including said base instruction set; and
at least one user-customized extension instruction within said instruction set;
wherein each of said modes provides unique functionality with respect to the other three
modes.

10 41. (Cancelled)

42. (Previously presented) The digital processor of Claim 40, wherein first and second of said at least four modes implement one- and two-cycle stalls within said pipeline, respectively.

43. (Currently amended) The digital processor of Claim ~~40~~ 42, wherein at least one
15 of said at least four modes operates without respect to a branch displacement metric.

44.-52. (Cancelled)

53. (New) The processor of Claim 37, wherein said bits of said branch instruction comprise two data bits defining four discrete modes controlling said execution, said execution further being controlled without regard to a branch direction metric.

20 54. (New) The processor of Claim 37, wherein at least one of the particular combinations of said bits of said branch instruction and the logical functions associated therewith are adapted for assignment by a user.

55. (New) The processor of Claim 53, wherein at least one of the particular combinations of said bits of said branch instruction and the logical functions associated
25 therewith are adapted for assignment by a user.

56. (New) The processor of Claim 38, wherein each of said four discrete modes is constrained to only one of a plurality of unique combinations of said plurality of bits.

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57. (New) The processor of Claim 38, wherein at least one of the particular combinations of said bits of said branch instruction and the logical functions associated therewith are adapted for assignment by a user.

58. (New) The processor of Claim 56, wherein at least one of the particular combinations of said bits of said branch instruction and the logical functions associated therewith are adapted for assignment by a user.

59. (New) An extended and user configured digital RISC processor having at least one pipeline comprising at least instruction fetch, decode, and execute stages, and an associated data storage device, wherein the execution of instructions within said at least one pipeline is controlled by the method comprising:

storing an instruction set within said data storage device, said instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said instruction words comprising a user-configurable branch instruction having a plurality of unique functional modes exclusively associated with respective ones of unique combinations of a plurality of mode control bits, said branch instruction directing branching to a first address within said data storage device;

assigning one of a plurality of values to each of said mode control bits of said at least one branch instruction;

decoding said at least one branch instruction including said assigned values;

determining whether to execute an instruction within said pipeline in a stage preceding that of said at least one branch instruction based at least in part on said assigned values;

branching to said first address based on said at least one branching instruction; and

performing, based at least in part on said act of decoding said assigned values, at least one other function dictated by the unique functional mode associated with said assigned values.

60. (New) A method of controlling the execution of instructions within an extended and user-configured pipelined RISC processor, comprising:

providing an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a

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jump instruction having at least one user-configurable mode and at least one user-definable mode associated therewith, said user-configurable and user-definable modes each being specified by the same ones of said plurality of data bits, said at least one user-definable mode not being predetermined in terms of function;

5 assigning one of a plurality of values to said ones of said data bits of said at least one jump instruction; and

controlling the execution of at least one subsequent instruction within said pipeline based on said one assigned value of said ones of data bits when said at least one jump instruction is decoded;

10 wherein said method further comprises generating a long immediate constant using a single word instruction by:

providing an instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits;

15 selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

storing said shifted immediate value in a register.

20 61. (New) A method of controlling the execution of instructions within an extended and user-configured pipelined RISC processor, comprising:

providing an instruction set comprising a plurality of instruction words, each of said instruction words comprising a plurality of data bits, at least one of said words comprising a jump instruction having at least one user-configurable mode and at least one user-definable
25 mode associated therewith, said user-configurable and user-definable modes each being specified by the same ones of said plurality of data bits, said at least one user-definable mode not being predetermined in terms of function;

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assigning one of a plurality of values to said ones of said data bits of said at least one jump instruction; and

controlling the execution of at least one subsequent instruction within said pipeline based on said one assigned value of said ones of data bits when said at least one jump

5 instruction is decoded; and

wherein at least one of said plurality of instruction words comprises an op-code, a plurality of fields each comprising a plurality of bits, and at least one short immediate value comprising a plurality of bits, said at least one instruction word being encoded according to the method comprising:

10 associating a first of said fields with a first data source;

associating a second of said fields with a second data source; and

performing a logical operation using said first and second data sources as operands, said logical operation being specified by said op-code;

15 wherein said at least one instruction word is used to generate a long immediate constant according to the method comprising:

selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

20 storing said shifted immediate value in a register.

62. (New) A user-configured and extended RISC processor comprising:

a processor core having a multistage instruction pipeline, said core being adapted to decode and execute instruction words;

a data interface between said processor core and an information storage device; and

25 an instruction set comprising a plurality of said instruction words, at least one of said instruction words being a user-configurable jump instruction containing data defining a plurality of jump delay slot modes and at least one user-defined mode, said jump delay slot modes and at least one user-defined mode each being specified by the same portions of said data, said at least

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one user-defined mode not being predetermined in terms of function, said plurality of modes controlling the execution of instructions within said instruction pipeline of said processor core in response to said at least one jump instruction word within said instruction set;

wherein said processor is further adapted to generate a long immediate constant using a
5 single word instruction by:

providing an instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits;

selecting a portion of said plurality of bits of said at least one short immediate
10 value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and storing said shifted immediate value in a register.

63. (New) A user-configured and extended digital processor comprising:

15 a processor core having a multistage instruction pipeline, said core being adapted to decode and execute instruction words;

a data interface between said processor core and an information storage device; and

an instruction set comprising a plurality of said instruction words, at least one of said instruction words being a user-configurable jump instruction containing data defining a plurality
20 of jump delay slot modes and at least one user-defined mode, said jump delay slot modes and at least one user-defined mode each being specified by the same portions of said data, said at least one user-defined mode not being predetermined in terms of function, said plurality of modes controlling the execution of instructions within said instruction pipeline of said processor core in response to said at least one jump instruction word within said instruction set;

25 wherein said at least one of said plurality of instruction words comprises an op-code, a plurality of fields each comprising a plurality of bits, and at least one short immediate value comprising a plurality of bits, said at least one instruction word being encoded by:

associating a first of said fields with a first data source;

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associating a second of said fields with a second data source; and
performing a logical operation using said first and second data sources as
operands, said logical operation being specified by said op-code; and
wherein said at least one instruction word is used to generate a long immediate constant

5 according to the method comprising:

selecting a portion of said plurality of bits of said at least one short immediate
value;

shifting all of said bits of said at least one short immediate value using said op-
code and only said portion of bits to produce a shifted immediate value; and

10 storing said shifted immediate value in a register.